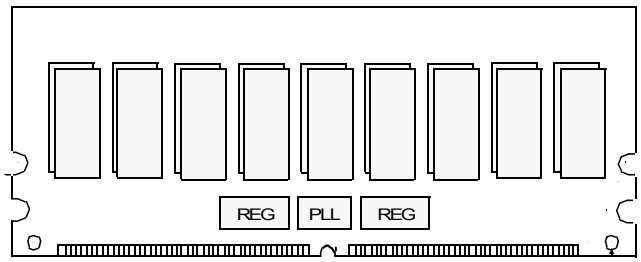
MACROTRON

MS41284L12872DR-07

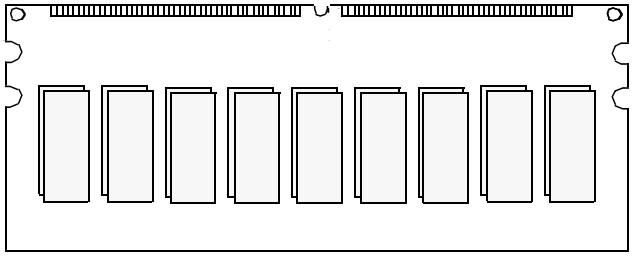
1 GB DDR SDRAM Module

128Mb x 72,184-Pin DIMM
2.5V DDR BUFF/REG SDRAMs with SPD

FRONT VIEW



BACK VIEW



GENERAL DESCRIPTION

The Macrotron MS41284L12872DR-07 is an 128M bit x 72 bit DDR266 Synchronous Dynamic RAM high speed buffered / registered memory module.
It consists of 18 CMOS 128M x 4 bit Double Data Rate Synchronous DRAMs in TSOP packages and a 2K EEPROM in 8-pin TSOP package on a 184-pin glass-epoxy substrate. Decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The product is a Dual In-line Memory Module and is intended for mounting into 184-pin edge connector sockets.

Synchronous design allows precise cycle controls with the use of system clock. Range of operating frequencies and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- 128 Megabit by 72 bit (1 Gigabyte) Synchronous DDR266 DRAM Module
- JEDEC-standard 184-pin, dual in-line memory module (DIMM)
- Error Correction Code (ECC) Capability
- Buffered/Registered
- 2.5V +/- 0.2V VDD and VDDQ Power Supply
- Fully differential clock operations (CK& $\overline{CK}$)
- Internal four bank operations with single pulsed RAS
- Auto refresh and self refresh supported
- Programmable burst lengths: 2,4 or 8 with both sequential and interleave mode
- Self Refresh and Auto Refresh Modes
- Serial Presence Detect (SPD)

PART NUMBER DESIGNATOR

MS 4 1284 A 12872 DR -07

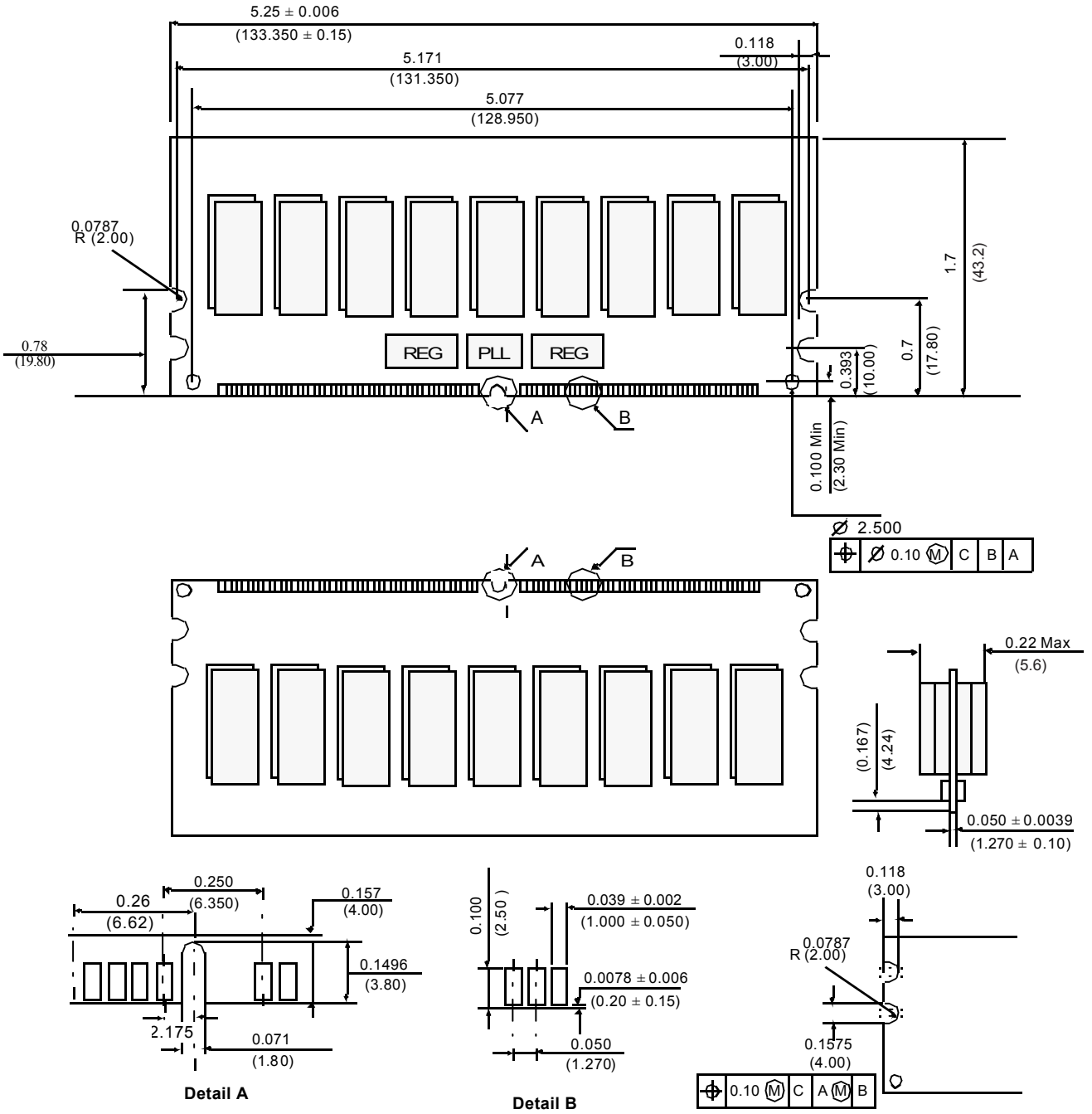
- -07 — Module Speed (uses 7.5ns DDR)
- DR — DDR Synchronous Registered
- 12872 — Module Configuration of 128 Mb x 72 bit
- A — PCB Revision
- 1284 — SDRAM Configuration of 64 Mb x 8 bit
- 4 — 184-Pin DIMM
- MS — Macrotron Systems

KEY TIMING PARAMETERS

PARAMETER	VALUE	UNIT
Module Bus Speed	266	MHz
Module Speed	7.5	ns
Clock Frequency	133	MHz
CAS Latency	2.5	Clock

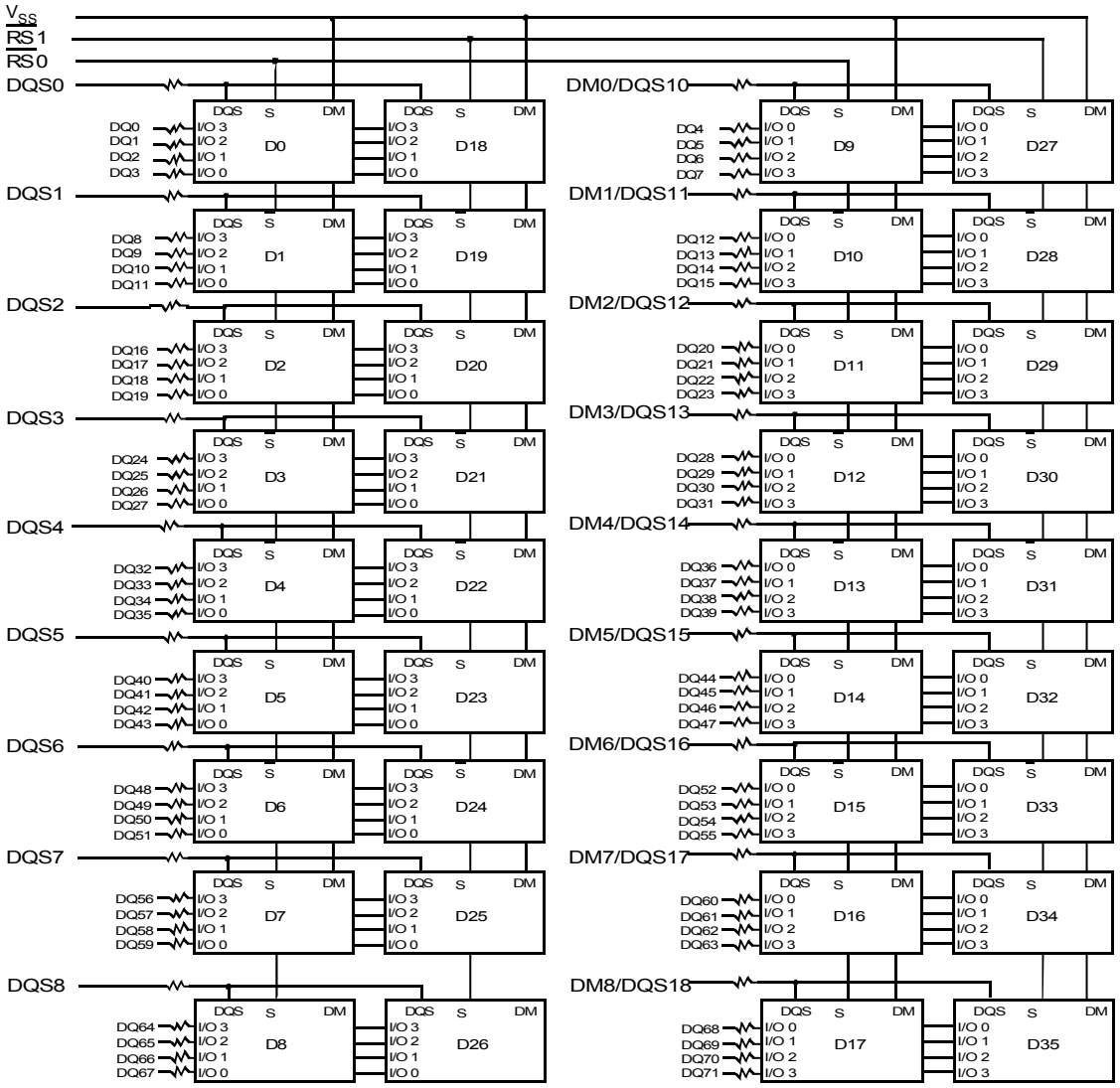
PACKAGE DIMENSIONS

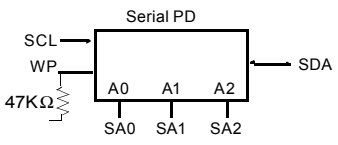
Units : Inches (Millimeters)

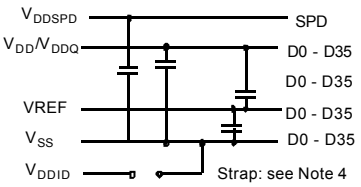


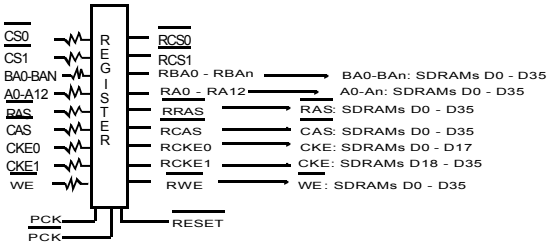
Tolerances : ± 0.005(.13) unless otherwise specified

Functional Block Diagram









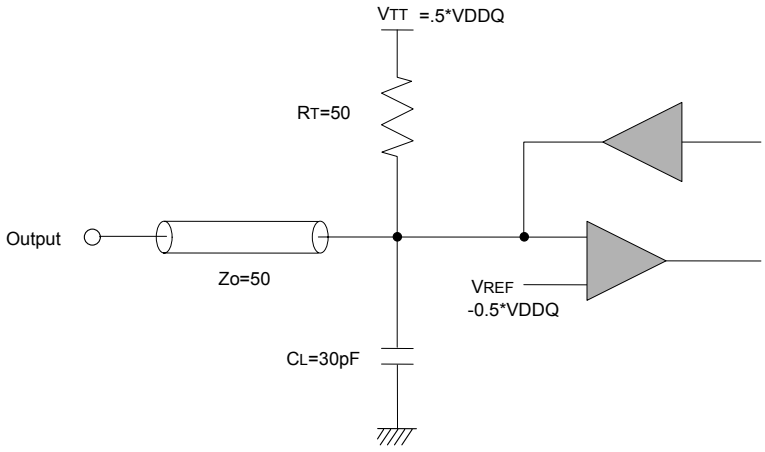
Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.

CAPACITANCE (TA=25°C, f=100MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input Capacitance	A0 ~ A12, BA0, BA1	CIN1	6	8	pF
Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	CIN2	6	8	pF
Input Capacitance	CKE0, CKE1	CIN3	5	7	pF
Input Capacitance	CS0, CS1	CIN4	5	7	pF
Input Capacitance	CK0, $\overline{CK0}$, CK1, $\overline{CK1}$, CK2, $\overline{CK2}$	CIN5	8	10	pF
Input Capacitance	DM0 ~ DM8	CIN6	12	14	pF
Data Input / Output Capacitance	DQ0 ~ DQ63, DQS0 ~ DQS8	CIO1	12	14	pF
Data Input / Output Capacitance	CB0 ~ CB7	CIO2	12	14	pF

Note :
1. VDD = 2.5 , VDDQ = 2.5V
2. Pins not under test are tied to GND.
3. These values are guaranteed by design and are tested on a sample basis only.

OUTPUT LOAD CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	^oC
Storage Temperature	T_{STG}	-55 ~ 125	^oC
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 3.6	V
Output Short Circuit Current	I_{OS}	50	mA
Power Dissipation	P_D	18	W
Soldering Temperature / Time	T_{SOLDER}	260 /10	^oC / Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITIONS (T_A=0 to 70 ^oC, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
Power Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V	1
Input High Voltage	V_{IH}	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	
Input Low Voltage	V_{IL}	-0.3	-	V_{REF} - 0.15	V	2
Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	
Reference Voltage	V_{REF}	0.49 xV_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	3

Note :
1. V_{DDQ} must not exceed the level of V_{DD}.
2. V_{IL} (min) is acceptable -1.5V AC pulse width with ≤ 5ns of duration.
3. The value of V_{REF} is approximately equal to 0.5 x V_{DDQ}.

AC OPERATING CONDITIONS (T_A=0 to 70 ^oC, Voltage referenced to V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	V_{REF} + 0.31		V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	$V_{IL(AC)}$		V_{REF} - 0.31	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX(AC)}$	0.5 xV_{DDQ}-0.2	0.5 x V_{DDQ}+0.2	V	2

Note :
1. VID is the magnitude of the difference between the input level on CK and the input on CK.
2. The value of V IX is expected to equal 0.5 xVDDQ of the transmitting device and must track variations in the DC level of the same.

PIN DESCRIPTION

Pin	Pin Description	Pin	Pin Description
CK0,/CK0,CK1,/CK1,CK2,/CK2	Differential Clock Inputs	VDDQ	DQs Power Supply
CS0, CS1	Chip Select Input	VSS	Ground
CKE0, CKE1	Clock Enable Input	VREF	Reference Power Supply
/RAS, /CAS, /WE	Commend Sets Inputs	VDDSPD	Power Supply for SPD
A0 ~ A12	Address	SA0~SA2	E^2PROM Address Inputs
BA0, BA1	Bank Address	SCL	E^2PROM Clock
DQ0~DQ63	Data Inputs/Outputs	SDA	E^2PROM Data I/O
CB0~CB7	Check Bit	WP	Write Protect Flag
DQS0~DQS7	Data Strobe Inputs/Outputs	VDDID	VDD Identification Flag
DM0~8	Data-in Mask	DU	Do not Use
VDD	Power Supply	NC	No Connection

PIN ASSIGNMENT

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	$\overline{CAS}$	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	$\overline{CS1}$
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	VSS	42	Vss	72	DQ48	103	A13*	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	$\overline{CK2}$	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	$\overline{CK0}$	168	VDD
16	CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	$\overline{CK1}$	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2*	144	CB7	174	DQ60
22	VDDQ	Key		83	DQ56	114	DQ20	Key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	WP	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

* These are not used on this module but may be used for other module in 184pin DIMM family